

CLAIM REVISIONS

1 1. (previously presented) A signal router, comprising:
2 a conditioning circuit configured to write K identical images of a first set
3 of data from N inputs to K random access memories during a first time interval;
4 K respective bit selectors each configured to read respective portions of a
5 respective one of said K identical images;
6 said K respective bit selectors being coupled to construct M output data
7 streams during a second time interval
8 wherein each of the random access memories comprises exactly two parts
9 configured so that during the second time interval a read occurs from a first one of the
10 parts, while a write occurs to a second one of the parts.

1 2. (canceled)

1 3. (previously presented) A signal router, as in claim 1, wherein said conditioning
2 circuit includes a buss to which said first set of data is applied and addressing
3 controllers configured to write data from said buss to said random access
4 memories, whereby said K identical images are written.

1 4. (previously presented) A signal router, comprising:
2 a controller programmed to store identical images of data from said N inputs in K
3 memories;

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4 said controller being further programmed to read respective bits of said data from
5 each of said K memories to produce M respective output data streams, whereby N inputs
6 are mapped to M outputs,

7 wherein each of the K memories comprises exactly two parts configured so that
8 during the second time interval a read occurs from a first one of the parts, while a write
9 occurs to a second one of the parts.

1 5. (currently amended) A router as in claim 4, further comprising a data buss
2 connected to receive said N inputs and distribute them to said K memories,
3 wherein pre-sorting of the input data is not necessary.

1 6. (currently amended) A router as in claim 5, wherein a bit rate of each of said ~~K~~-M
2 output streams is less than a bit rate of said buss.

1 7. (Previously presented) A method of routing data from N inputs to M outputs,
2 comprising the steps of:
3 applying data from said N inputs to a data buss by means of at least one of
4 time and space multiplexing;
5 imaging said data on K random access memories from said buss;
6 reading respective sets of bits from said random access memories to form
7 respective ones of said signals ultimately demultiplexed to form said M outputs,
8 wherein each of the random access memories comprises exactly two parts
9 configured so that during the second time interval a read occurs from a first one of the
10 parts, while a write occurs to a second one of the parts.

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1 8. (previously presented) The router of claim 1, wherein the parts are configured so that upon
2 completion of the second interval, the first and second parts change roles, so that subsequently
3 the first part is used for the write and the second part is used for the read.

1 9. (previously presented) The router of claim 4, wherein the parts are configured so that upon
2 completion of the second interval, the first and second parts change roles, so that subsequently
3 the first part is used for the write and the second part is used for the read.

1 10. (previously presented) The method of claim 7, wherein the parts are configured so that upon
2 completion of the second interval, the first and second parts change roles, so that subsequently
3 the first part is used for the write and the second part is used for the read.

1 11. (currently amended) A signal router, comprising:
2 • N inputs for receiving synchronous streams of serial broadcast data;
3 • a conditioning circuit configured to write K identical images of a first set of data from the N
4 inputs to K memories during a first time interval;
5 • K respective bit selectors each configured to read respective portions of a respective one of
6 said K identical images; and
7 • each of said K respective bit selectors being coupled to construct M output data streams
8 during a second time interval.